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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,252	06/28/2000	Raminda U. Madurawe	A293D	5633

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/606,252	MADURAWE ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27,29-31,33-38,40 and 42-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27,29-31,33-38,40 and 42-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 3, 2004 have been approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 27, 29 – 31, 33, 34, 35 – 38, 40, and 42 – 44 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

It is not clear where in the originally filed specification support for "wherein the first and second pocket implants are entirely between a source region and a drain region" [emphasis added] can be found. The originally filed written description on page 3, lines 11 – 14 describes the pocket implants of the present invention "extend into the channel region between the source region and the drain region to cause a reverse short channel effect for the transistor." Since the pocket implants "extend into the channel region between the source region and the drain region" they must exist in some other region that is not entirely between the source and drain regions.

Further, on page 6, lines 32 – 35 of the originally filed specification the formation and location of pocket implants are described: "Pocket implants 310 may be implemented through large angle implantation. They surround the junctions of source/drain regions 105." The description of the pocket implants surrounding "the junctions of source/drain regions 105" at least describes the pocket implants as overlapping the edges of the source/drain regions. Since they overlap these junction edges of the source/drain regions, they must exist in at least a portion of a region of the source/drain regions. Therefore the pocket implants would not be considered to be "entirely between a source region and a drain region" in the present invention. While a broad interpretation of the figures might be used to argue that this limitation exists in the originally filed specification, in all of the figures showing pocket implants, it is clear that the pocket implants extend at least partially in a vertical direction below a region where either the source or drain region exists. This region would not be considered "between a source region and a drain region". Therefore the figures also do not show first and second pocket implants that are "entirely between a source region and a drain region".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 27, 29, 30, 31, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (USPAT 5763921, Okumura) in view Yuki et al. (USPAT 5466957, Yuki) and Sanchez (USPAT 5583067).

With regard to claim 27, Okumura discloses in figures 2 – 7 a method of fabricating a transistor in an integrated circuit device. Okumura discloses in figure 2 providing a semiconductor substrate (1). Okumura discloses in figure 6 implanting a field implant (63). Okumura discloses in figure 5 implanting a well implant (62). Okumura discloses in figure 4 implanting an enhancement implant (61). Okumura discloses in figure 7 forming a gate oxide (7) on the semiconductor substrate. Okumura discloses in figure 7 forming a gate (8) on the gate oxide. Okumura discloses in figures 4 – 7 a source region (10b) and a drain region (10a). Okumura does not teach pocket implants. Yuki teaches in figure 3b implanting (22) a first pocket implant (right side 21a) into the semiconductor substrate from a first side of the gate. Yuki teaches in figure 3b implanting a second pocket implant (left side 21a) into the semiconductor substrate from a second side of the gate. As far as the examiner can ascertain, Yuki teaches in figure 3b – 3d wherein (at least a portion of) the first and second pocket implants are entirely between a source region (right 26/27) and a drain region (left 26/27). Yuki further teaches in figure 3b – 3d wherein first pocket implant and the second pocket implant are in contact at about the center of a channel region. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the pocket implants of Yuki in the method of Okumura in order to suppress short channel effect while reducing the electric field concentration as stated by Yuki in column 1, lines 47 – 51 and column 4, lines 31 – 41. The pocket implants of Yuki result in an excellent semiconductor device, as Yuki states in column 4, lines 31 – 41. Yuki teaches in

column 5, lines 54 – 60 that the pocket implants are boron implants. Okumura and Yuki are silent to the fact that the first pocket implant and the second pocket implant laterally diffuse in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Okumura and Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45.

With regard to claim 29, Yuki teaches in figure 3b the first pocket implant and the second pocket implant are implanted at an angle.

With regard to claim 30, Yuki teaches in figure 3b the first pocket implant and the second pocket implant are implanted using the gate as a mask.

With regard to claim 31, it should be noted that "wherein the diffusing increases a reverse short channel effect of the transistor" is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Okumura, Yuki, and Sanchez read on the claimed invention.

With regard to claim 33, Yuki teaches in figure 3a – 3d; column 5, lines 51 – 67; and column 6, lines 1 – 11 forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.

With regard to claim 34, Yuki teaches in figure 3b – 3d; column 5, lines 51 – 67; and column 6, lines 1 – 11 that the first polarity is different than the second polarity.

6. Claims 35, 36, 38, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuki in view of Sanchez.

With regard to claim 35, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21). Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate using the gate as a mask. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. Yuki is silent to the first pocket implant and the second pocket implant laterally diffusing in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. As far as the examiner can ascertain, Yuki teaches in figure 3b – 3d wherein (at least a portion of) the first and second pocket implants are entirely between a source region (right 26/27) and a drain region (left 26/27).

With regard to claims 36, it should be noted that "wherein the diffusing increases a threshold voltage of the transistor" is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

With regard to claim 38, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21) having a surface. Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate surface. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate from the first side of the gate at an angle. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. Yuki is silent to the first pocket implant and the second pocket implant laterally diffusing in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. As far as the examiner can ascertain, Yuki teaches in figure 3b – 3d wherein (at least a portion of) the first and second pocket implants are entirely between a source region (right 26/27) and a drain region (left 26/27).

With regard to claim 40, Yuki discloses in figure 3b wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

With regard to claim 42, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21). Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate from the first side of the gate at an angle. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. Yuki is silent to the first pocket implant and the second pocket implant laterally diffusing in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. As far as the examiner can ascertain, Yuki teaches in figure 3b – 3d wherein (at least a portion of) the first and second pocket implants are entirely between a source region (right 26/27) and a drain region (left 26/27).

With regard to claims 43, it should be noted that "wherein the diffusing increases a threshold voltage of the transistor" is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

7. Claim 37 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuki and Sanchez as applied to claims 35 and 42, respectively, above, and further in view of Okumura.

Yuki and Sanchez teach forming transistors with pocket implants. Yuki and Sanchez do not disclose implanting an enhancement implant. Okumura teaches in figure 6 implanting an enhancement implant (63) in the semiconductor substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the enhancement implant of Okumura in the method of Yuki and Sanchez in order to control the threshold voltage of the device as stated by Okumura in column 6, lines 56 – 62.

Response to Arguments

8. Applicant's arguments filed May 14, 2004 have been fully considered but they are not persuasive.

9. With regard to applicant's argument that "Sanchez strongly advocates not using implants 16 since implants 16 do not surround the entire drain," it should be noted that Sanchez is used to teach diffusing a boron implant. Further, Sanchez is good for all that it teaches, even if there is a suggestion that one or more of those features are not always desirable. A reference cannot teach away from itself, for example: two references should be used in a "teaching against" argument

(i.e. reference A teaches against reference B). Finally, because the present originally filed specification does not have support for the claimed subject matter of "wherein the first and second pocket implants are entirely between a source region and a drain region" no arguments directly relating to this limitation are given considerable weight. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II